Using Routing Techniques to Minimize Skew

Although my name does not appear on the byline for this article, I was in truth the author. I was given a PowerPoint presentation and an audio cassette tape (of a similar, but different presentation), and asked to come up with a draft of this trade journal article. The biggest challenge was that I knew almost nothing about printed circuit boards when I started. It was literally Greek to me. However, by listening to the cassette several times and asking questions, I was able to come up with a draft. With only minor tweaks, that draft became the submitted article.

I also worked with the authors to develop the graphics, which included suggesting places where a picture would be helpful, giving feedback on the graphics they started with, and advising them on formats that the journal would accept.

For this article and several others, I also served as the Platform Technology Lab Group's "publishing advisor." I helped them understand such principles as editorial calendars and guidelines, printing processes (and the several weeks required for printing), and submission and query procedures.

This PDF is a black-and-white drawing, to conserve bandwidth. If you would like the full-color version, please feel free to contact me.

Using routing techniques to minimize skew

Faster designs leave smaller tolerances

BY BRYCE HORINE AND MIKE LEDDIGE

As bus designs get faster and faster, printed circuit board tolerances for skew get proportionately smaller. For example, a Direct RDRAM channel can deliver data at up to 400 MHz, while allowing a total of only 125 picoseceonds of interconnect skew. Thus, proper routing techniques are crucial to the design of PCBs such as Direct RDRAM. By paying critical attention to design strategy, you can incorporate routing procedures that remove systematic sources of skew from your design.

Some of the techniques that are especially useful in memory system design include minimizing the number and severity of bends in the lines, minimizing line discontinuities by reducing neck-down, using exact trace length matching to minimize timing skew due to routing, matching the number of vias on each line, and using ground shielding for signal trace separation. These same techniques can be applied to RIMM modules or other high-speed designs.

Managing the number and type of signal line bends

In the ideal Direct RDRAM board design, all the lines on the board are the same length without any bends, matching both the physical length and the electrical delay of the lines. To achieve this goal, or to come as close as possible, you need to manage the number and types of bends carefully. This includes the following:

- reducing the total number of bends;
- using angles of 45° or less; and
- minimizing the number of small or closely spaced bends.

Reducing the total number of bends

All too commonly, in order to meet physical length-matching requirements, PCB routing resembles a plate of spaghetti. Even though the physical length of the lines may be matched with the addition of bends in the lines, it is very difficult to match the electrical delay exactly, because each bend introduces .3 to .5 ps of electrical delay. Since matching the electrical delay of the lines is as important as matching the physical length of the lines in Direct RDRAM design, you will always want the fewest bends possible. **Figure 1** illustrates typical "spaghetti" routing, and **Figure 2** depicts the desired smooth routing. Note that the placement of the components has remained the same in the two figures. Only the routing was modified to minimize the number of bends.

Because of the wide traces associated with low impedance boards such as Direct RDRAM motherboards (typically 14 to 19 mils wide), it is especially important to minimize bends. Electrical current tries to cut the corner around each bend instead of flowing uniformly across a trace. This tendency is illustrated by Line A in **Figure 3**. In this diagram, the electrical delay (indicated by the large dotted line) is somewhat longer than the measured length given by the CAD tool (indicated by the smaller dotted line).

However, Line A is a better scenario than Line B, where the bends are so close together that the current shoots straight through. In this case, the difference between the measured physical length and the electrical delay is even greater than in Line A.

Using angles of 45° or less

Where a bend is unavoidable, use nothing larger than 45°. If you stick to 45° or less, the difference

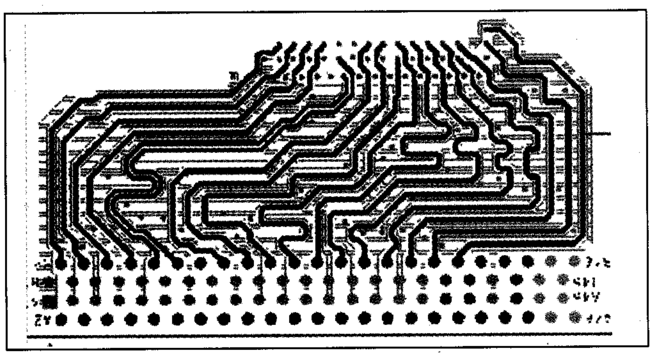


Figure 1—*Typical "spaghetti" routing*

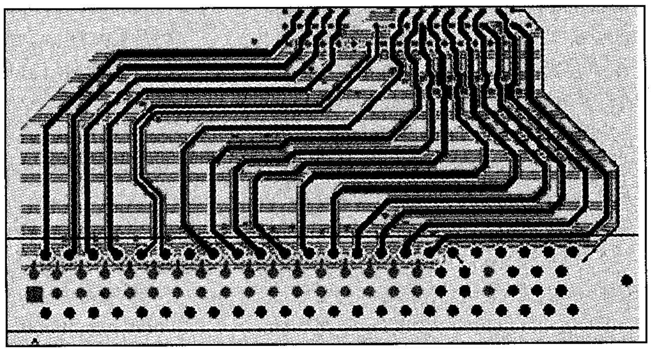


Figure 2—*An example of smooth "river routing"*

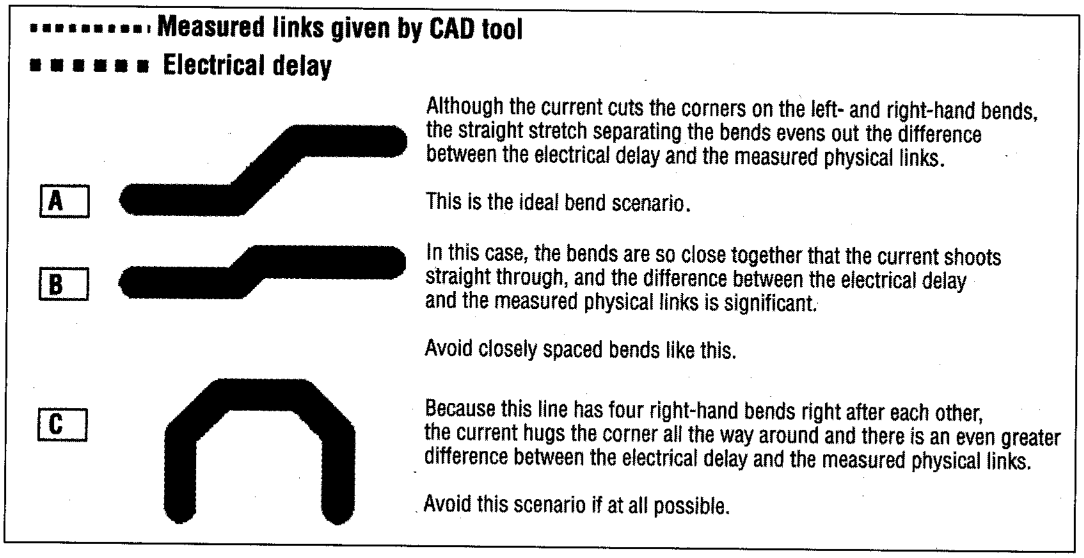


Figure 3—*Example of current cutting the corner on bends*

between the electrical delay and the physical length of the line will be minimized. (Although your CAD tool may indicate a physical length change, this is negligible.) If you need to make a large bend, such as 90°, "round" the corner by using two 45° bends with a straight section in between.

Minimizing the number of small or closely spaced bends

Where possible, avoid using tiny bends that are spaced closely together. For example, Line C in Figure 3 has four right-hand bends immediately after one another. In this case, the difference between the electrical delay of the line and the measured length is quite large.

Of course, designing a board with fewer bends in the lines takes longer, and one bend by itself will not break the bus timing. However, the effect of bends is cumulative, and two or three hours of effort spent reducing the number of bends pays off with a robust system design that more efficiently uses the board's real estate and improves electrical performance.

Minimizing discontinuities in the line by reducing neck-down

Every time you neck-down a trace, you introduce a discontinuity in the line that degrades the electrical performance of the board. While you cannot avoid neck-downs entirely, you can minimize their effect with a bit of extra effort.

When squeezing a wide trace between two vias, such as in the component escape area or between two connector pins, you may need to reduce the trace width. This changes the impedance of the trace, introducing a discontinuity. To minimize this effect, keep the neck-down as short as possible, as shown in **Figure 4**. (Standard practice is to neck-down a trace until it is has escaped the component area.)

You may be tempted to neck-down the trace when routing through the RIMM connector pin field. By choosing a bend angle other than 45°(the standard angle), you can reduce the number of necessary neck-downs as shown in **Figure 5.** As mentioned previously, angles of 45° do not significantly affect the electrical performance of the line. Another possible benefit of using angles 45° or smaller is the shortening of the trace length while minimizing the number of bends. Angles other than 45° are not hard to do; you simply need to slightly adjust your CAD tool settings.

Using exact trace length-matching

To further reduce signal-to-signal

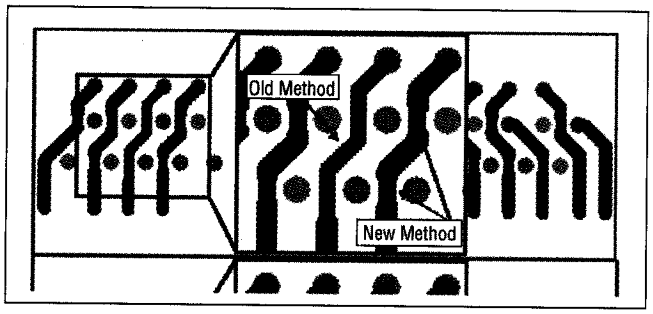


Figure 4—*Example of reducing neck-down*

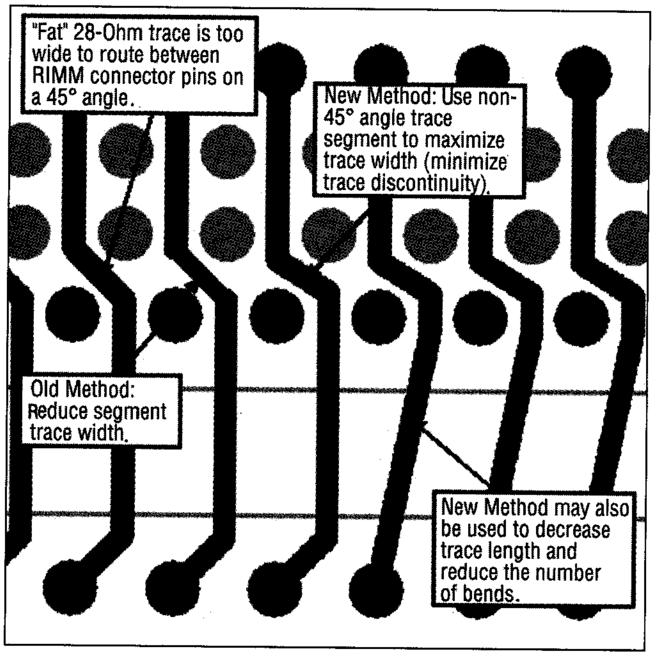


Figure 5—*Using non-45° angles to minimize line discontinuities*

Using routing techniques
continued

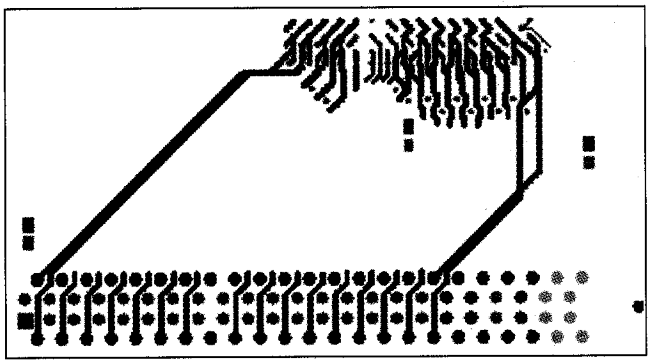


Figure 6—*Routing outside lines before length-matching to longest line*

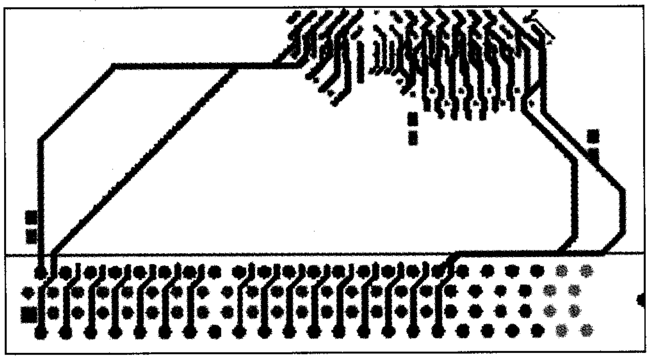


Figure 7—*Lines expanded to match longest routed length*

skew, you must be vigilant in trace length-matching for same-layer and layer-to-layer wiring, including the vertical path through the vias. This means you also must exactly match the pad capacitance at the controller by adding vias at every RDRAM signal.

When length-matching the Direct Rambus channel, utilizing the following procedure will optimize your layout design. Start by connecting the two outside traces on each routing layer, as shown in **Figure 6.** Then look for the longest trace, and stretch the other traces to match, as shown in **Figure 7**.

This example defines the routing area. Route all the remaining traces within this area. **Figure 8** shows the final result of using this length-matching technique on one routing layer. Note the uniformity of the line spacing and the smoothly turning signals that result from using this procedure.

If you break down the routing task section by section, length-matching is not that difficult. To meet specs, your length matching must be within ±10mils. With some additional effort, designs have been completed that match traces within 0.4 mils.

Via matching

Another way to maximize the performance of the board by minimizing layer-to-layer skew is to match the number and type of vias on every line to account for via delay differences. This requires the insertion of vias on all lines, regardless of top or bottom layer escape, to equalize the loading and delay differences. This has been verified through extensive lab measurements showing that first-order compensation of top and bottom PCB delay differences is achieved through via placement. Ideally, you should have the same number of vias on each line and make sure each via crosses the same number of PCB layers.

As previously mentioned, every line does not require a via. To obtain the best electrical performance, a "dummy" via is placed on the trace, whether or not a trace requires a via for routing purposes, as shown in **Figure 9**. (A dummy via stays on the same layer, unlike a real via, which takes a signal from one layer to another.)

Even though the dummy via does not have exactly the same electrical delay as a real via, a dummy via is better than no via on the trace at all. If possible, you should have the same number of dummy and real vias on each line.

Using ground shielding for signal trace separation

Crosstalk is a common source of skew. One method of reducing crosstalk is to widely space the signal lines. However, to significantly reduce the crosstalk, you need spacings of 40 to 50 mils, which waste a lot of routing real estate. A better technique involves using ground shielding to isolate lines, as shown in **Figure 10**. This saves a great deal of room on the board, typically 20 mils per line. Where

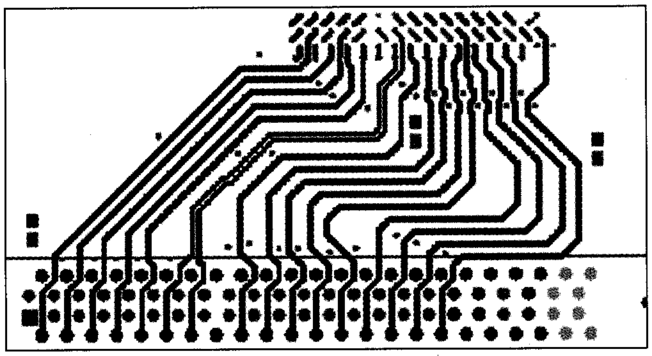


Figure 8—*Length-matched RDRAM routing*

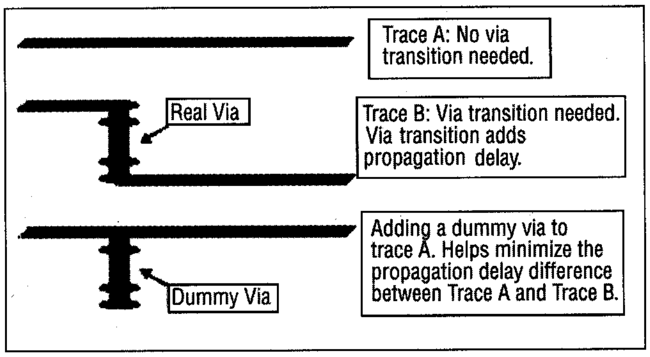


Figure 9—*Example of adding a "dummy" via to a trace*

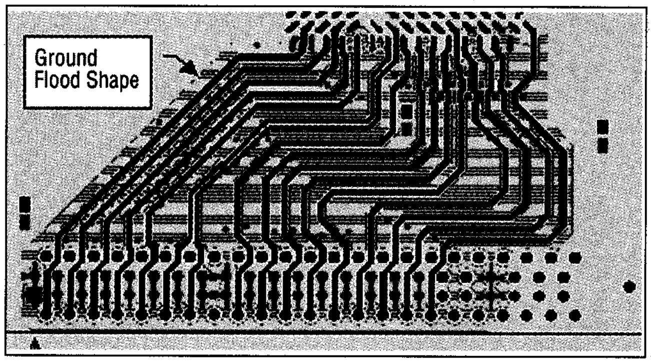
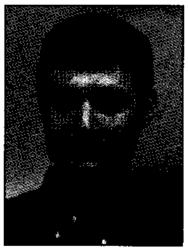


Figure 10—*Routed RDRAM channel with ground flood shape*

there are no signal lines, you should flood that area with ground and then connect the ground flood shape to the ground plane with vias. This helps further reduce crosstalk and keeps the ground planes tied down better. Also, using the ground flood shape lets you use a slightly narrower line by lowering the trace impedance.

Conclusion

All the techniques described in this article use today's PCB technology. They do not require any special tools or new manufacturing methods. Careful attention to detail is all that is required to eliminate all systematic sources of design skew. As in life itself, the "devil" is in the details. ■



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Resources

For more information on designing motherboards and RIMM modules for Direct RDRAM, visit the following Intel and RAMBUS Web sites:

http://developer.intel.com/design/chipsets/memory/rdram.htm

http://www.rimm.com